

AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

1. (Currently Amended) A data sequence conversion circuit which takes as an input any one of a plurality of input data sequences having different data widths, and which converts said input data sequence into an output data sequence having a prescribed data width for output, said circuit comprising:

a first parallel shift register ~~for holding said input data sequence~~ that receives parallel input data having a first data width, wherein the first parallel shift register receives a sequence of data elements respectively having the first data width and holds the sequence of data elements together in the first parallel shift register;

a switch matrix ~~for taking~~ receiving the data held in said first parallel shift register as input data, and ~~for~~ outputting said input data in a distributed fashion in accordance with a rule selected by a control signal from a plurality of predetermined rules; and

a second parallel shift register ~~for taking~~ receiving the data output from said switch matrix as input data, and ~~for~~ outputting said input data as a data sequence having said prescribed data width parallel output data having a second data width different from the first data width, wherein the second parallel shift register outputs said input data as a sequence of data elements respectively having the second data width.

2. (Original) A data sequence conversion circuit as claimed in claim 1, wherein when the data widths of said plurality of input data sequences are denoted by W_n ($n = 1, 2, 3, \dots$), respectively, and the data width of said output data sequence by W_o , said first parallel shift register has a data width at least equal to the largest value of W_n ($n = 1, 2, 3, \dots$), and has the number of stages at least equal to the largest value of the quotients Q_{In} ($n = 1, 2, 3, \dots$) each obtained by dividing the least common multiple of W_n ($n = 1, 2, 3, \dots$) and W_o by W_n .

3. (Original) A data sequence conversion circuit as claimed in claim 1, wherein when the data widths of said plurality of input data sequences are denoted by W_n ($n = 1, 2, 3, \dots$), respectively, and the data width of said output data sequence by W_o , said second parallel shift register has the number of stages at least equal to the largest value of the quotients Q_{On} ($n = 1, 2, 3, \dots$) each obtained by dividing the least common multiple of W_n ($n = 1, 2, 3, \dots$) and W_o by W_o .

4. (Original) A data sequence conversion circuit as claimed in claim 1, wherein the data widths of said plurality of input data sequences are 5 bits, 4 bits, and 3 bits, respectively, the data width of said output data sequence is 8 bits, said first parallel shift register has a 5-bit data width and eight stages, and said second parallel shift register has five stages.

5. (Original) A data sequence conversion circuit as claimed in claim 1, wherein when the data width of said input data sequence is denoted by W_n , and the data width of said output data

sequence by W_o , said switch matrix outputs said input data so that $W_n \times Q_{In}$ units of data input and held in the first stage to the (Q_{In}) th stage in said first parallel shift register as counted from the input side thereof are input to the first stage to the (Q_{On}) th stage in said second parallel shift register as counted from the output side thereof, where Q_{In} is the quotient of the least common multiple of W_n and W_o divided by W_n , and Q_{On} is the quotient of the least common multiple of W_n and W_o divided by W_o .

6. (Original) A data sequence conversion circuit as claimed in claim 1, wherein when the data width of said input data sequence is denoted by W_n , and the data width of said output data sequence by W_o , the shift clock frequency F_i of said first parallel shift register and the shift clock frequency F_o of said second parallel shift register have a relation defined by $F_i/F_o = W_o/W_n$.

7. (Original) A data sequence conversion circuit as claimed in claim 1, wherein when the data width of said input data sequence is denoted by W_n , and the data width of said output data sequence by W_o , each time Q_{In} data sequences are input into said first parallel shift register, $W_n \times Q_{In}$ units of data are input into said second parallel shift register via said switch matrix, following which Q_{On} data sequences are output from said second parallel shift register.

8. (Original) A printer comprising a data sequence conversion circuit as claimed in claim 1, said data sequence circuit being located between a jaggy correction circuit and a line-like printhead.